REMARKS

Claims 1-16, 21-22 and 24-26 are pending. By this amendment, claims 1, 10, 16, 24 and 25 are amended and claim 26 has been added. Support for the amendments to claims 1, 16 and 24 can be found in Figs. 2c-2j and the language in the specification describing the same. No new matter has been added. Applicants respectfully request reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

Allowed Claims

Applicants appreciate the indication that claims 10-12 contain allowable subject matter and would be allowed if presented in independent form. As claim 10 has been presented in independent form and as claims 11 and 12 depend from claim 10, Applicants respectfully request that at least claims 10-12 be indicated to be allowed. Moreover, Applicants submit that all claims are in condition for allowance for the following reasons.

35 U.S.C. §112, 1st paragraph, Rejection

Claim 24 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. This rejection is moot and/or respectfully traversed.

While Applicants disagree with the Examiner's assertions and interpretation of the claims, by this Amendment, Applicants submit that this basis of rejection has been

rendered moot. Applicants note that support for forming the bird's beak in the gate polysilicon finds support in, among other places, the specification and original claim 1.

For example, the paragraph bridging pages 3 and 4 of the specification and original claim 1 disclose that, after oxidizing step of the gate polisilicon, a bird's beak is formed.

Accordingly, Applicants respectfully request that this basis of rejection be withdrawn.

35 U.S.C. §112, 2nd paragraph, Rejection

Claim 24 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite on the basis of the Section 112, first paragraph, rejection. This rejection is moot and/or respectfully traversed.

By this Amendment, Applicants submit that this basis of rejection has been rendered moot. Again, support for forming the bird's beak in the gate polysilicon finds support in, among other places in the specification and original claim 1.

Accordingly, Applicants respectfully request that this basis of rejection be withdrawn.

35 U.S.C. §102(e) Rejection

Claims 1, 2, 16, 24 and 25 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No.: 6,573,172 to EN, *et al.* ("EN"). This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because EN fails to teach each and every element of the claims.

More particularly, amended independent claims 16 and 24 recites, *inter alia,*

> forming oxide or a first oxide between a side of a gate polysilicon and a spacer of the n-type transistor or the n-type field effect transistor.

Additionally, amended independent claim 1 further recites, *inter alia,*

> removing, after the oxidizing step, oxide formed during the oxidizing step from above the gate polysilicon of the n-type transistor,
> wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon between the gate polysilicon and a spacer and the removing step preserves the bird's beak.

Moreover, amended independent claim 16 further recites, *inter alia,*

> removing oxide formed during the oxidizing step from above the gate polysilicon of the n-type field effect transistor,
> wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon between the gate polysilicon and the spacer and wherein the removing step preserves the bird's beak

Additionally, amended independent claim 24 further recites, *inter alia,*

> removing the first oxide from above the gate polysilicon of the n-type transistor while allowing the first oxide to remain between the side of the gate polysilicon and the spacer,
> removing the oxide formed during the oxidizing from above the gate polysilicon of the n-type transistor,
> wherein, after the removing of the oxide formed during the oxidizing, a bird's beak remains in the gate polysilicon between the gate polysilicon and the spacer of the n-type transistor.

Applicants submit that EN does not disclose, or even suggest, at least these features.

Applicants acknowledge, for example, that Figs. 2G and 2H of EN show how a mask 160 is utilized to cover a nitride layer 150 above an NMOS device 102 while a second nitride layer 150 is removed from oxide layer 140 of the PMOS device 104. Applicants also acknowledge that EN discloses that the "resulting structure" shown in Fig. 2H creates "a tensile stress in the channel region 116 of the NMOS transistor 102" (see col. 7, 50-56). However, it is clear that this document does not specifically disclose or suggest that the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon between the gate polysilicon and a spacer of the n-type transistor wherein the removing step preserves the bird's beak. Nor is there any apparent disclosure with regard to forming oxide or a first oxide between a side of a gate polysilicon and a spacer of the n-type transistor or of the n-type field effect transistor. To the contrary, the figures of EN do not show any bird's beak or any oxide formed between a side of the polysilicon gate 108 and the spacers 112. Nor has the Examiner demonstrated otherwise.

It is also clear that this document does not specifically disclose or suggest removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor. Applicants note, in particular, that col. 7, lines 36-39 of EN specifically indicates that "the oxide layer 140 serves as an etch-stop layer for the etch process ...". Thus, EN provides for removing the second nitride layer 150 and not the oxide layer 140 while the NMOS is masked. EN clearly does not disclose the removal of the oxide layer 140 from above the gate polysilicon of the n-type transistor.

Moreover, while the Examiner has alleged that EN discloses the formation, by an oxidizing step, of a bird's beak in an edge of the gate polysilicon, the Examiner has failed to identify any such structure in EN or any language in EN which would support this position. The Examiner has simply failed to identify any such structure that is arranged within the gate polysilicon of the n-type field effect transistor.

Finally, Applicants dispute the Examiner's assertions that because EN discloses depositing of an oxide layer 140 on the gate 108, that this "would necessarily result in formation of a bird's beak in an edge of the gate polysilicon". This statement is not correct and mis-characterizes Applicants' disclosure. As the Examiner will note, the instant invention, as shown in e.g., Figs. 2g-2i, utilizes an oxide 15 between the gate polysilicon and the spacers 26. This oxide 15 is arranged between the gate polysilicon and the spacers 26 during the oxidizing step and during the formation of a bird's beak. EN, on the other hand, does not provide for any oxide between the spacers 112 and the gate polysilicon 108. Thus, the Examiner cannot properly argue that the oxidizing step in EN would *per se* result in the formation of a bird's beak in the device disclosed in EN.

Thus, for the above-noted reasons, Applicants respectfully submit that independent claims 1, 16 and 24, and claims 2 and 25, which depend from claims 1 and 24, are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn.

35 U.S.C. § 103 Rejections

Claims 1, 6-9, 13-16, 21, 22, 24 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,204,103 issued to BAI, *et al.* ("BAI") in view of EN. Claims 3-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over EN in view of U. S. Patent No. 6,491,981 issued to CHANG, *et al.* ("CHANG"). These rejections are respectfully traversed.

The Examiner has acknowledged on page 7 of the instant Office Action that BAI lacks any disclosure or suggestion with regard to the covering, oxidixing and removing steps. However, the Examiner explains that EN discloses these features and that it would have been obvious to combine the teachings of these documents. The Examiner also acknowledged on pages 10 and 11 of the instant Office Action that EN lacks any disclosure or suggestion with regard to the features recited in claims 3-5. However, the Examiner explains that CHNG discloses these features and that it would have been obvious to combine the teachings of these documents.

Applicants have clearly demonstrated above that EN also lacks a number of features recited in claims 1, 16 and 24, and respectfully submit that no proper combination of BAI and EN or EN and CHANG disclose or suggest the combination of features recited in claims 1, 16 and 24.

As explained above, while EN discloses how a mask 160 is utilized to cover a nitride layer 150 above an NMOS device 102 while a second nitride layer 150 is removed from oxide layer 140 of the PMOS device 104, and discloses that the "resulting

structure" shown in Fig. 2H creates "a tensile stress in the channel region 116 of the NMOS transistor 102" (see col. 7, 50-56), EN does not does not specifically disclose or suggest forming oxide or a first oxide between a side of a gate polysilicon and a spacer of the n-type transistor or of the n-type field effect transistor. Again, the figures of EN clearly do not show any oxide formed between a side of the polysilicon gate 108 and the spacers 112. Nor has the Examiner demonstrated otherwise.

Moreover, EN is also entirely silent with regard to removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor. As noted above, col. 7, lines 36-39 of EN specifically indicates that "the oxide layer 140 serves as an etch-stop layer for the etch process ...". Thus, EN provides for removing the second nitride layer 150 and not the oxide layer 140 while the NMOS is masked. EN clearly does not disclose the removal of the oxide layer 140 from above the gate polysilicon of the n-type transistor. Moreover, while the Examiner has alleged that EN discloses the formation, by an oxidizing step, of a bird's beak in an edge of the gate polysilicon, the Examiner has failed to identify any such structure in EN. The Examiner has failed to identify any such structure that is arranged within the gate polysilicon of the n-type field effect transistor. Accordingly, Applicants submit that EN fails to cure the deficiencies of BAI which were clearly acknowledged by the Examiner to be missing from BAI.

With regard to BAI, Applicants submits that it is clear from the figures that BAI is also entirely silent with regard to forming oxide or a first oxide between a side of a gate polysilicon and a spacer of the n-type transistor or of the n-type field effect transistor. Nor has the Examiner shown otherwise.

Finally, with regard to CHANG, Applicants acknowledge that this document discloses a process of oxidizing a polysilicon layer 24a with a operating temperature from 550 to 750 degrees C. (see col. 3, lines 27-34). However, it is clear that CHANG fails to disclose or suggest any masking steps, much less, removing an oxide layer. It is also clear that CHANG lacks any disclosure with regard to creating a tensile stress in the channel of a n-type transistor. Additionally, CHANG does not does not contain any disclosure with regard to removing, after the oxidizing step, oxide above the gate polysilicon of a n-type transistor. Finally, Applicants submit that CHANG is also entirely silent with regard to forming oxide or a first oxide between a side of a gate polysilicon and a spacer of the n-type transistor or of the n-type field effect transistor. Thus, CHANG also fails to cure the deficiencies of EN.

Applicants also submit that the dependent claims are distinguishable over the applied documents:

Claims 3-15, 21, 22 and 24 are allowable over the cited references based on their dependencies from an allowable base claim. Additionally, claims 14 and 15 are further allowable based on their additional features.

Claims 14 and 15 recite that the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create a stress of about 700MPa in a channel of the n-type field effect transistor or about 500Pa to about 1000Pa. The Examiner maintains that the claimed tensile stress ranges lack criticality because Applicants do not teach that the tensile stress ranges solve any stated problem or are for any particular purpose. Applicants again respectfully traverse this submission, and direct the Examiner's attention to Figures 4 and 5, as well as to page 2 of the

specification, where it is stated that tensile stresses in conventional n-type devices are relatively moderate (i.e., for example, about 200 MPa to about 300 MPa). Comparing the results of Figures 4 and 5 to these conventional results, it is seen that embodiments of the present invention offer improved tensile stress ranges, which are in embodiments are critical to their operation.

Additionally, Applicants further direct the Examiner's attention to page 10 of the specification, where it is noted:

> the oxidation of the gate of the NFETs creates large tensile stresses in the channel region of the NFETs ... Further, these tensile stresses increase electron mobility along the channel, and improve the performance of the NFETs.

At page 13, it is noted that the desired stresses are tensile and add values of the order of 200MPa and above. For these reasons, and because the cited references disclose a tensile stress of about 100 MPa, the tensile stress ranges recited in claims 14 and 15 are allowable. Consequently, allowance of claims 14 and 15 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required.

Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458**.

Respectfully submitted,
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